CLAIMS

What is claimed is:

1. A method for implementing a programmable chip system, the method comprising:

receiving customization information associated with a processor core and a plurality of programmable chip components;

configuring the processor core and the plurality of programmable chip components for implementation on the programmable chip;

determining voltage and ground pins associated with the programmable chip;

providing a netlist, wherein a printed circuit board layout tool uses the netlist to generate a layout coupling the processor core and the plurality of programmable chip components to off-chip components.

2. The method of claim 1, wherein the netlist is a printer circuit board netlist.

3. The method of claim 2, wherein capacitors are bypassed for ground pints and voltage pins.

4. The method of claim 1, wherein the plurality of programmable chip components are received from a library.

5. The method of claim 1, wherein customization information includes parameterization information.

6. The method of claim 1, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

7. The method of claim 1, wherein the off-chip component is an external memory device.

8. The method of claim 1, wherein the off-chip component is an application specific standard product.

9. The method of claim 8, wherein the printed circuit board layout tool takes the netlist and generates schematic traces.

10. A system for implementing a programmable device, the system comprising:

an interface operable to receive customization information associated with a processor core and a plurality of programmable chip components;

a processor operable to configure the processor core and the plurality of programmable chip components for implementation on the programmable chip, the processor configured to determine voltage and ground pins associated with the programmable chip and provide a netlist to a printed circuit board layout tool, wherein the printed circuit board layout tool uses the netlist to generate a connection layout coupling the processor core and the plurality of programmable chip components to off-chip components.

11. The system of claim 10, wherein the netlist is a printer circuit board netlist.

12. The system of claim 11, wherein capacitors are bypassed for ground pints and voltage pins.

13. The system of claim 10, wherein the plurality of programmable chip components are received from a library.

14. The system of claim 13, wherein customization information includes parameterization information.

15. The system of claim 14, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

16. The system of claim 10, wherein the off-chip component is an external memory device.

17. The system of claim 10, wherein the off-chip component is an application specific standard product.

18. The system of claim 17, wherein the printed circuit board layout tool takes the netlist and generates schematic traces.

19. An apparatus for implementing a programmable chip system, the apparatus comprising:

means for receiving customization information associated with a processor core and a plurality of programmable chip components;

means for configuring the processor core and the plurality of programmable chip components for implementation on the programmable chip;

means for determining voltage and ground pins associated with the programmable chip;

means for providing a netlist to a printed circuit board layout tool, wherein the printed circuit board layout tool uses the netlist to connect the processor core and the plurality of programmable chip components with the off-chip components.

20. The apparatus of claim 19, wherein the netlist is a printer circuit board netlist.

21. The apparatus of claim 20, wherein capacitors are bypassed for ground pints and voltage pins.

22. The apparatus of claim 19, wherein the plurality of programmable chip components are received from a library.

23. The apparatus of claim 19, wherein customization information includes parameterization information.

24. The apparatus of claim 19, wherein the processor core and the plurality of programmable chip components are connected using a simultaneously multiple primary component fabric.

25. The apparatus of claim 19, wherein the off-chip component is an external memory device.

26. The apparatus of claim 19, wherein the off-chip component is an application specific standard product.